REMARKS

The Final Office Action mailed on March 2, 2004, has been received and its contents carefully considered.

Claims 1 and 3-20 are currently pending in this application, with claims 1, 3, 4 and 8 being the independent claims.

The Applicants note with appreciation the Examiner's indication in the Final Action that claims 3, 6, 8, 10, 12-16 and 19 are allowed, and that claims 5 and 7 would be allowable if rewritten in independent form including all of the limitations of their respective base claims and any intervening claims.

In this Amendment, claims 1, 3, 4 and 8 are amended to more clearly reflect that the first electrode and the second electrode are formed as parts of the first integrated semiconductor chip and the second integrated semiconductor chip, respectively. It is respectfully submitted that the amendments herein to claims 1, 3, 4 and 8 do not change their scope or otherwise affect their allowability.

In the Final Action, claims 1, 4, 9, 11, 17-18 and 20 are rejected under 35 USC §103(a) as being obvious over *Akram* (U.S. Patent No. 6,297,547) in view of *Takeda* (U.S. Patent No. 6,414,381), and further in view of *Bezama et al.* (U.S. Patent No. 6,297,547). The rejection is respectfully traversed.

Regarding the rejected claims, the Examiner points to *Akram* as disclosing a mounting structure from multiple semiconductor dies in a package where a semiconductor device includes multiple dies, in which a first die and a second die are mounted on a lead frame. The bond pads on the first and second dies are wire-bonded to the lead frame. The first die, the second die and lead frame are encapsulated in a package. However, the Examiner acknowledges that *Akram* fails to disclose the required interposer structure and the required nonconductive interposer structure. To cure this deficiency in the *Akram* reference, the Examiner points to *Takeda* as disclosing an interposer for separating stacked semiconductor chips mounted on a multi-layer printed circuit board where the required interposer structure is disclosed. Further, the Examiner points to *Bezama* as disclosing a method and apparatus to manufacture and electronic package with direct wiring pattern where the required non-conducting interposer structure is disclosed. The Examiner argues

that it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the required interposer and the required non-conducting interposer structure in *Akram* as taught by *Takeda* and *Bezama*, respectively, in order to have a semiconductor packaging structure with smaller size.

The Applicants respectfully disagree with the Examiner's argument. In the invention defined by independent claim 1, a first integrated semiconductor chip is mounted back-to back on a second integrated semiconductor chip, and the second integrated semiconductor chip is mounted on a first surface of a nonconductive interposer substrate having a through-hole, such that a second electrode for wiring formed on the front side of the second chip is exposed through the through-hole to external terminals on the second surface of the interposer substrate. In the invention defined by independent claim 4, a first integrated semiconductor chip of a first chip size is mounted back-to back on a second integrated semiconductor chip of a second chip size, and the first integrated semiconductor chip is mounted on a first surface of a nonconductive interposer substrate having a through-hole that is smaller than the first chip size and larger than the second chip size, such that the through-hole is covered by the first chip and the back side of the first chip, to which the second chip is mounted, is exposed through the through-hole from a side of the interposer substrate at the interposer substrate second surface. *Akram* does disclose in Figures 1 and 2, for example, embodiments in which a first semiconductor die 20 and a second semiconductor die 30 are mounted back-to-back, with the first semiconductor die 20 being mounted in turn to either top surface 173 or bottom surface 174 of lead frame 170. As the Examiner acknowledges, however, *Akram* fails to disclose the nonconductive interposer substrate element recited in claim 1, or the interposer substrate element recited in claim 4.

The Examiner relies on *Takeda* for the interposer substrate element missing in *Akram*. However, what *Takeda* discloses is an interposer that holds the second semiconductor chip above the first semiconductor chip so that there is a separation between them while electrically connecting the second semiconductor chip and the multilayer printed circuit board on which the first chip is mounted (see Abstract). In the embodiment shown in Figure 5 of *Takeda*, for example, the interposer includes a lead frame 31A, wires 28B (first electrical connection parts) and wires 28C (second electrical connection parts). The lead frame 31A has stage 29A and a plurality of lead parts 30A and is made of a

material such as a 42-ally and a copper ally which are commonly used as material for leads of semiconductor devices (column 5, line 66 through column 6, line 4). Obviously, the interposer of *Takeda* in not non-conductive, as claim 1 would require. But, *Takeda* also fails to teach or suggest that the interposer has a through-hole through which the reverse side of the chip mounted on the interposer is exposed, as required in claim 4, or that the interposer has a through hole through which an electrode on the front side of the chip mounted on the interposer is exposed, as required in claim 1. There is no suggestion in *Takeda* of the interposer having any through-hole at all. Moreover, the interposer in *Takeda* is used in various configurations in which the semiconductor chips are mounted separately, one over the other (see Figures 5-8, for example), but in no instance are they disclosed as being mounted back-to-back.

The *Bezama* reference appears to add nothing relevant to the teachings of *Akram* and *Takeda*. *Bezama* is directed to an electronic package assembly that includes two electronic modules and an interposer having a top surface and a bottom surface, provided between the two electronic modules, where the top surface has a conductive array matching the external contacts of the first module and the bottom surface has a conductive array matching the external contacts of the second module, and the includes a plurality of conductors traversing a thickness of the interposer to connect the first and second conductive arrays (seeing Abstract). Although the interposer in *Bezama* may arguably be characterized as nonconductive, *Bezama* fails to disclose an interposer having a through-hole, as independent claims 1 and 4 specifically require. Moreover, like *Takeda*, *Bezama* fails to suggest the use of an interposer in the context of two chips mounted back-to-back.

Thus it appears that the Examiner has engaged in piecemeal reconstruction of the *Akram* patent, picking and choosing from the *Takeda* and *Bezama* references only so much of them as will support a given a position, to the exclusion of other parts necessary to the full appreciation of what these references fairly suggest to one of ordinary skill in the art. Even if the inventions of the references were combined as suggested by the Examiner, a structure having the features recited in the claims would not be achieved.

For at least the foregoing reasons, is respectfully submitted that claims 1, 4, 9, 11, 17-18 and 20 patentably distinguish over the applied art references, whether considered individually or in combination. The rejection accordingly should be withdrawn.

Based on the above, it is submitted that the application is in condition for allowance and notice of such, with allowed claims 1 and 3-20, is earnestly solicited.

Should the Examiner believe that a conference would help to expedite the prosecution of this application, the Examiner is encouraged to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

June 2, 2004
Date

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